Code: 9A04401

R09

B.Tech II Year II Semester (R09) Supplementary Examinations December/January 2014/2015

SWITCHING THEORY & LOGIC DESIGN

(Common to EEE, ECE, EIE, E.Con.E & ECC)

Time: 3 hours Max. Marks: 70

Answer any FIVE questions

All questions carry equal marks

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1 (a) Explain the ASCII code with table.

(b) Encode the following text in to 7-bit ASCII code:
JNTU ANANTAPUR

2 (a) Prove that OR-AND network is equivalent to NOR-NOR network.

(b) Simplify the following Boolean functions to minimum number of literals:
(i) x' + y' + xyz'
(ii) (x' + xyz') + (x' + xyz')(x + x'y'z)

(c) Realize XOR gate using minimum number of NAND gates.

3 (a) What are the advantages of Tabulation method over K-map?

(b) Simplify the following Boolean function using Tabulation method:
Y(A,B,C,D) = ∑(1,3,5,8,9,11,15)

4 (a) Design 4-bit even parity generator. Mention truth table.

(b) Design BCD to XS3 code converter using a 4 bit Full- adders MSI circuit.

5 (a) Find the minimal threshold-logic realization for the function:
f(A,B,C,D) = Σm(2, 3, 6, 7, 10, 12, 14, 15)

(b) Compare programmable logic devices.

6 With a neat sketch explain 4-bit Johnson counter

7 Find the equivalence partition and the corresponding reduce machine in standard form.

PS	NS_1Z	
	X = 0	X = 1
A	D,0	H,1
B	F,1	C,1
C	D,0	F,1
D	C,0	E,1
E	C,1	D,1
F	D,1	D,1
G	D,1	C,1
H	B,1	A,1

8 (a) Draw the ASM chart for binary divider.

(b) Draw the state diagram for a full adder circuit and convert it to ASM chart.

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